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Resolvendo os Gargalos do Edge

FPGAs: De monstros a solução

João Dullius
Engenheiro de Aplicações - BP&M

O palestrante

João Dullius
BP&M Representações
joaodullius@bpmrep.com.br

- Engenheiro de Aplicações
  - Processamento Embedded
  - FPGAs

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BROADCOM

AVAGO Authorized Representative

XILINX

Littelfuse

Micron

FINISAR

IDT

Pulse Electronics

Grayhill

TELINK SEMICONDUCTOR

GaN Systems

EVE

ZETTLER AMERICAN ZETTLER, INC.

NORTHFORGE

Internet of Everything

Qual a quantiade de dados gerada diariamente?

2.5 Exabytes
de dados gerados por dia

90% dos Dados do Mundo
gerados nos últimos 2 anos

Mais de 60 Yottabytes
serão usados em AI em 2019

Source: Forbes https://www.forbes.com/sites/bernardmarr/2018/05/21/how-much-data-do-we-create-every-day-the-mind-blowing-stats-everyone-should-read/#558a143f60ba

VoT - Video of Things®

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VoT - Video of Things®

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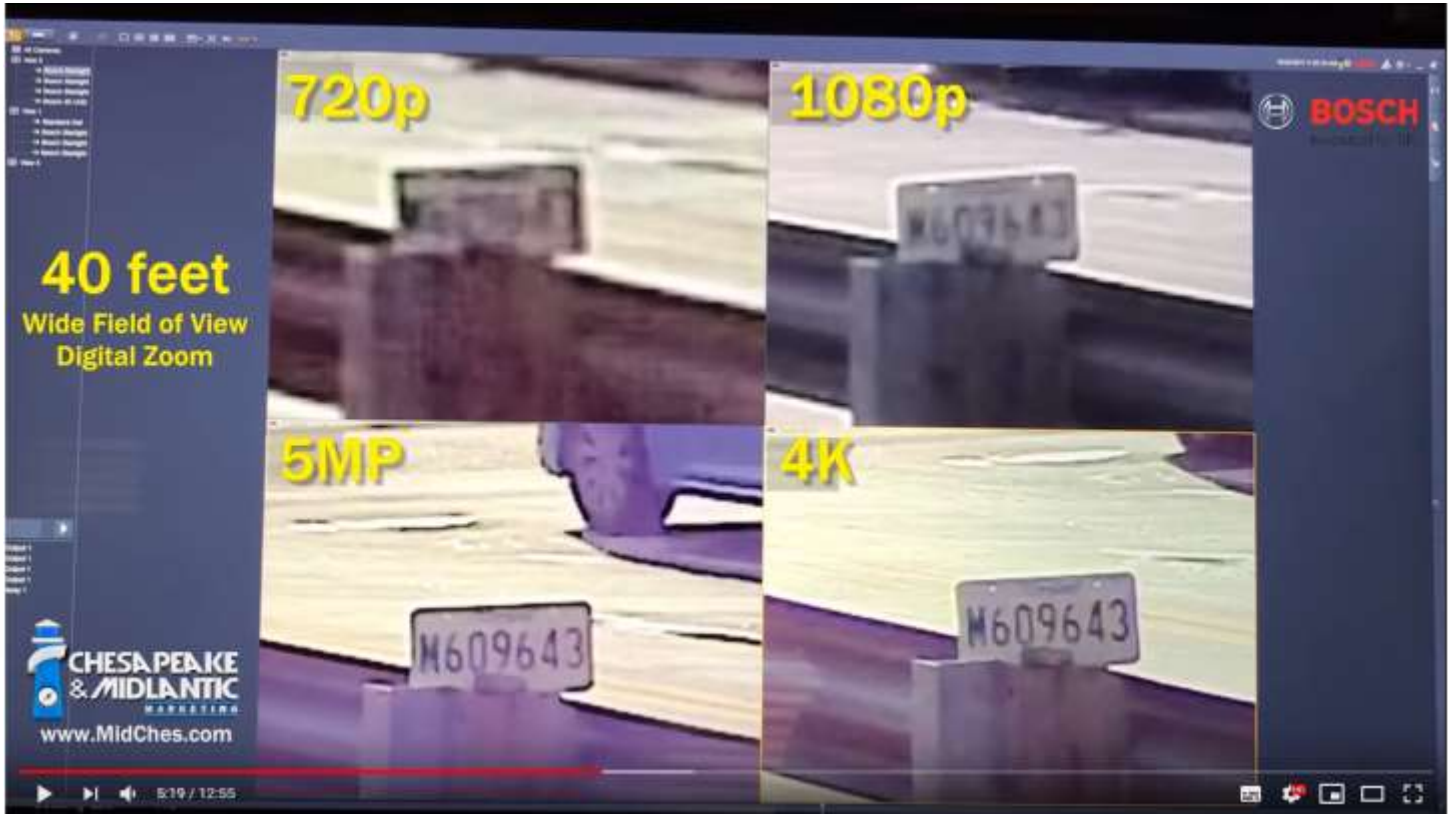

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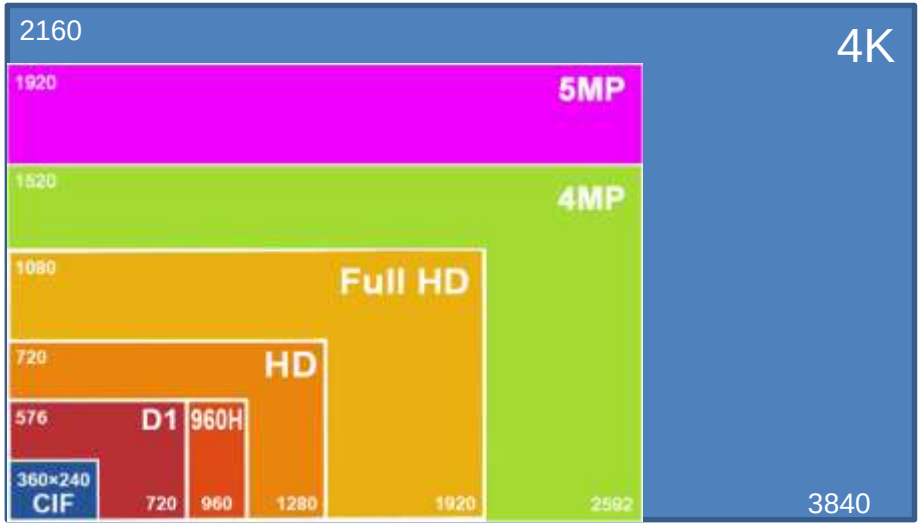

VoT - Video of Things®

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Resolution	H.264	MJPEG
1MP (1280*720)	2 Mbps per camera	6 Mbps per camera
2MP (1920*1080)	4 Mbps per camera	12 Mbps per camera
5MP (2560*1960)	10 Mbps per camera	30 Mbps per camera
4K (3840*2160)	18 Mbps per camera	64 Mbps per camera

Rede 4G

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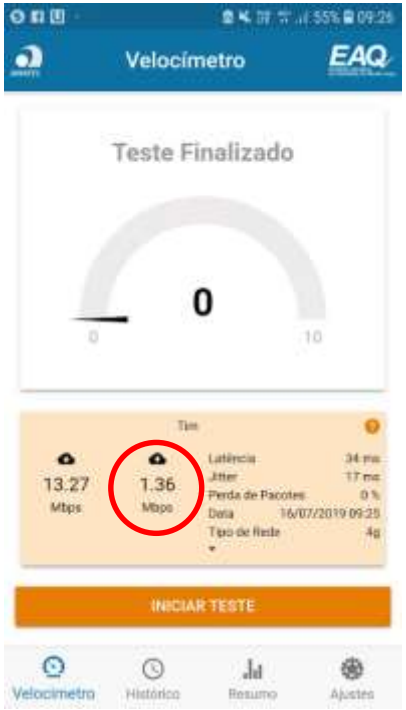
16/07/19

Palestra Yara Senger

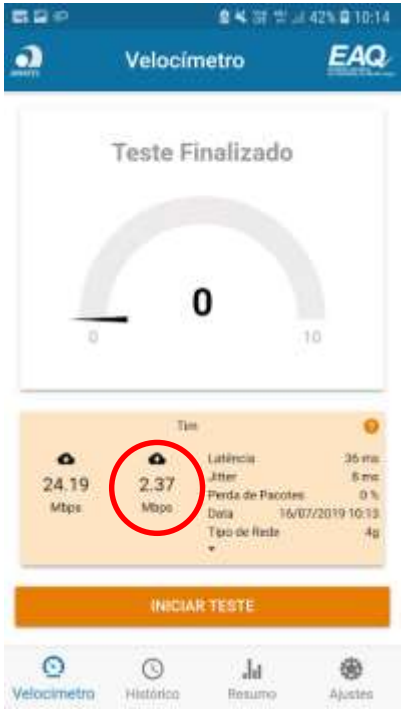
Sala Stadium



16/07/19

Palestra Alberto Cardoso

Sala IoT

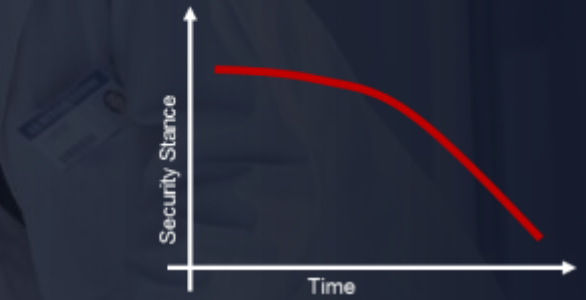


Privacidade de dados e Segurança

- Mais de **100M** de **devices IoT** na área medica estão **atualmente** instalados, crescendo para **161M** em **2020**
- Executivos dizem que **privacidade (59%)**, integração de sistemas **legados (55%)** e **segurança (54%)** são as três maiores barreiras travando a adoção de IoT na área médica atualmente

Privacidade de dados e Segurança

GDPR



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Privacidade de dados e Segurança

GDPR

Bolsonaro sanciona lei que cria autoridade de proteção de dados

Órgão será responsável por fiscalizar o uso de informações pessoais por empresas

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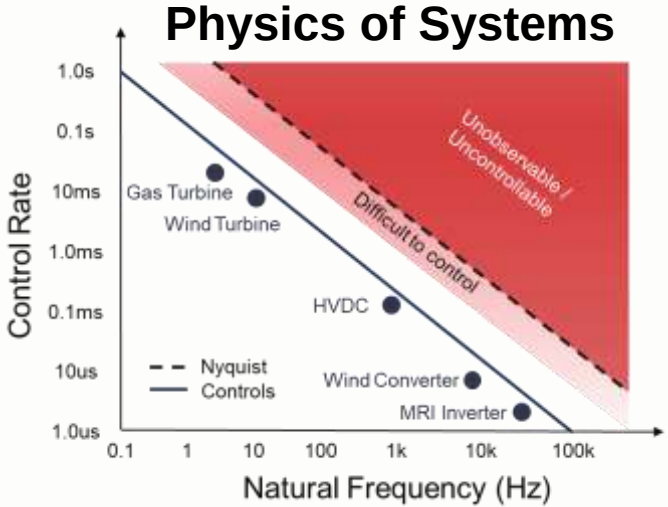
PoT - Physics of Things®



Distância NYC/LA: 2,800 milhas
Velocidade da luz: 186,000 milhas/s
Round trip: 2*2800/186000 = 30ms
Frequência de Controle = 10ms

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GARGALOS DE PROCESSAMENTO

AI Computer Vision

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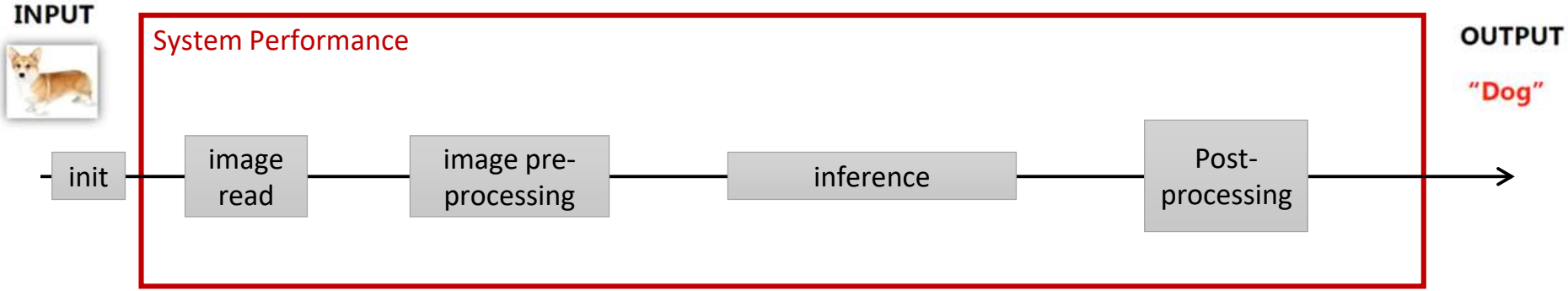

Goodbye Moore Law

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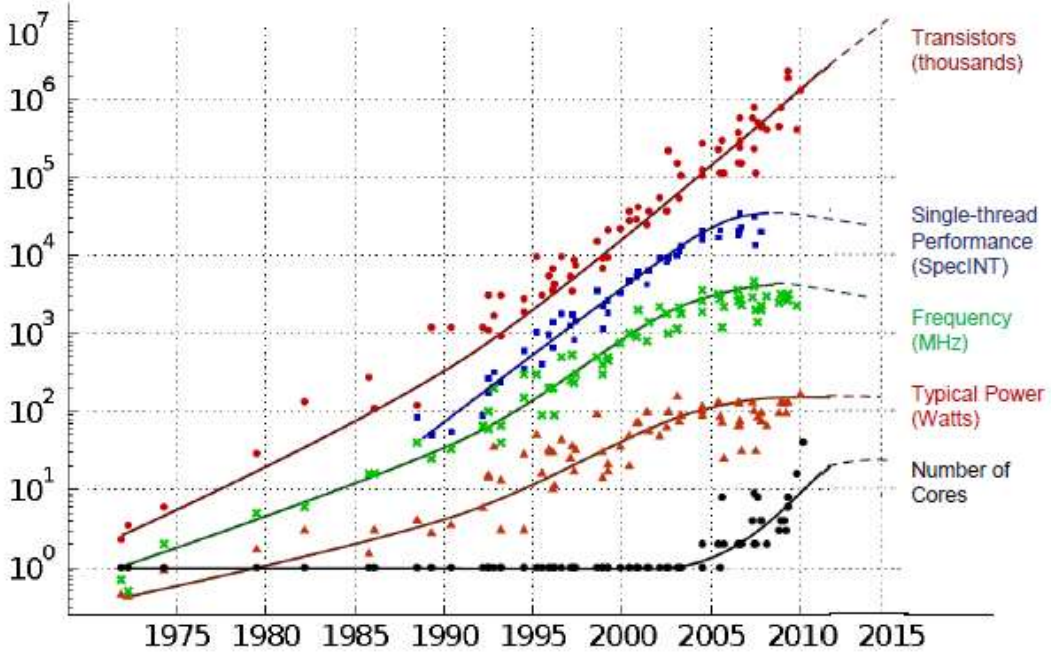
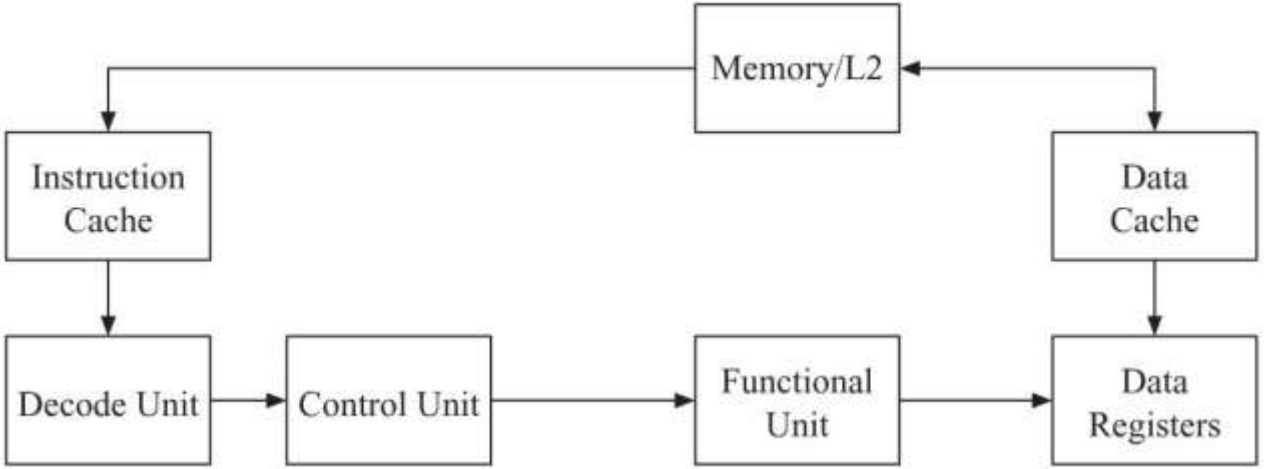


CPUs são sequenciais!



AI Computer Vision

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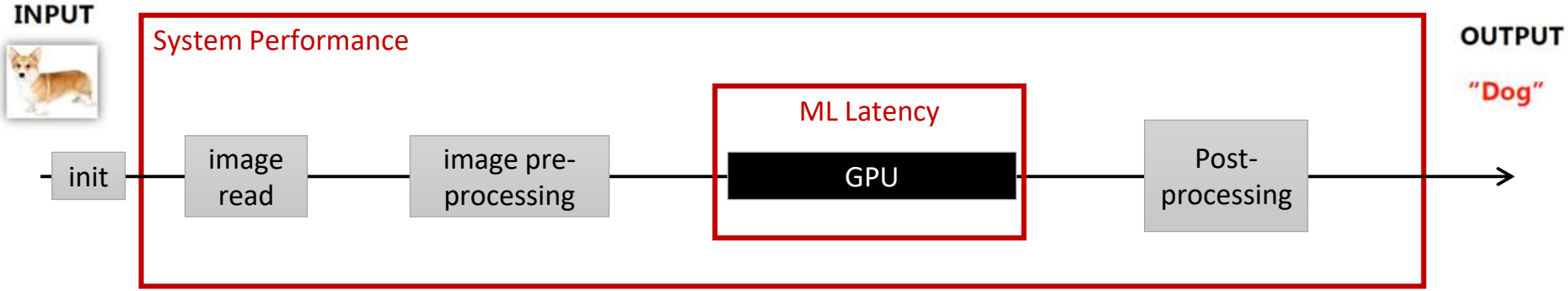

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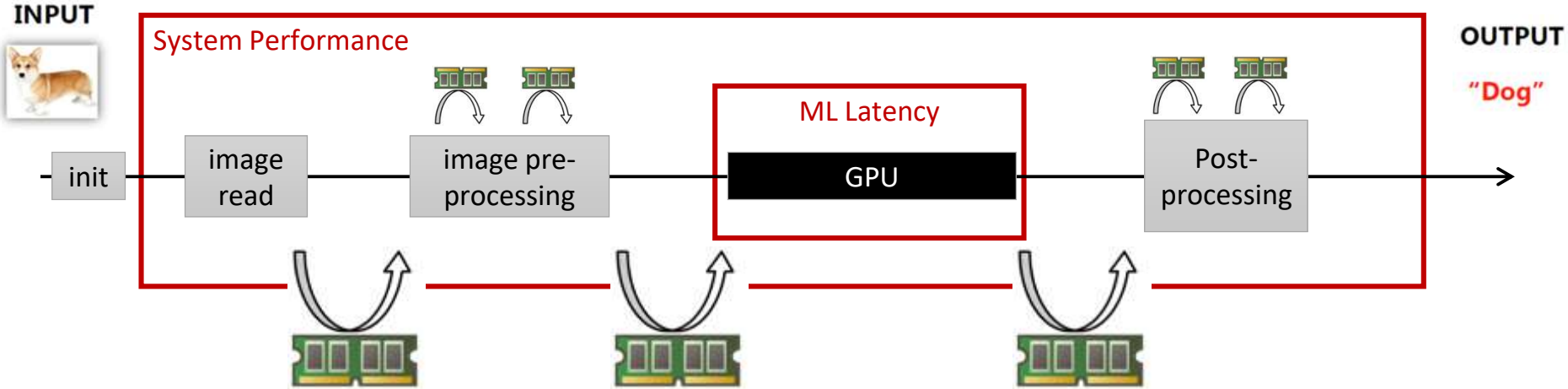

AI Computer Vision

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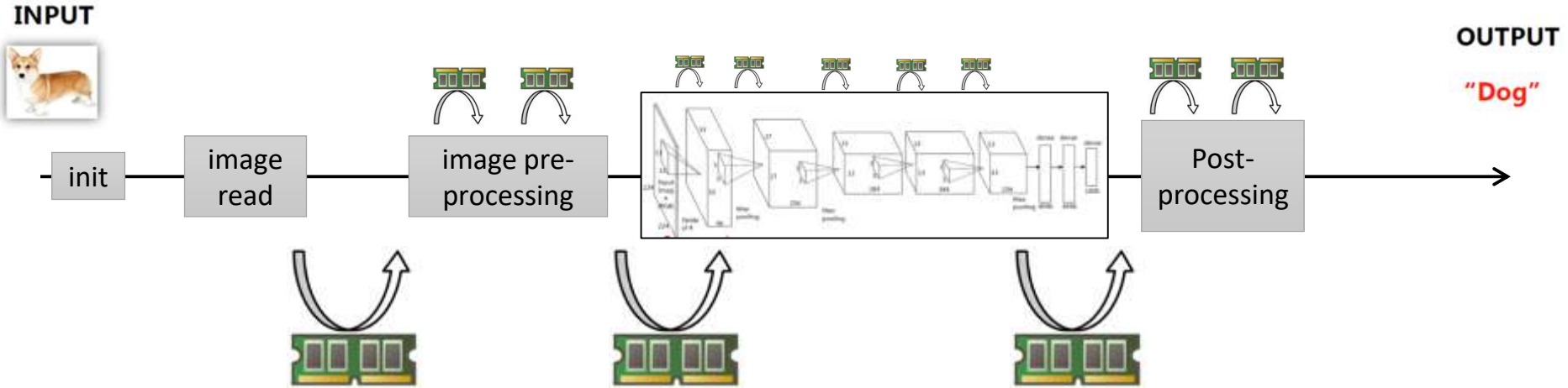

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FPGA

O Monstro

FPGAs

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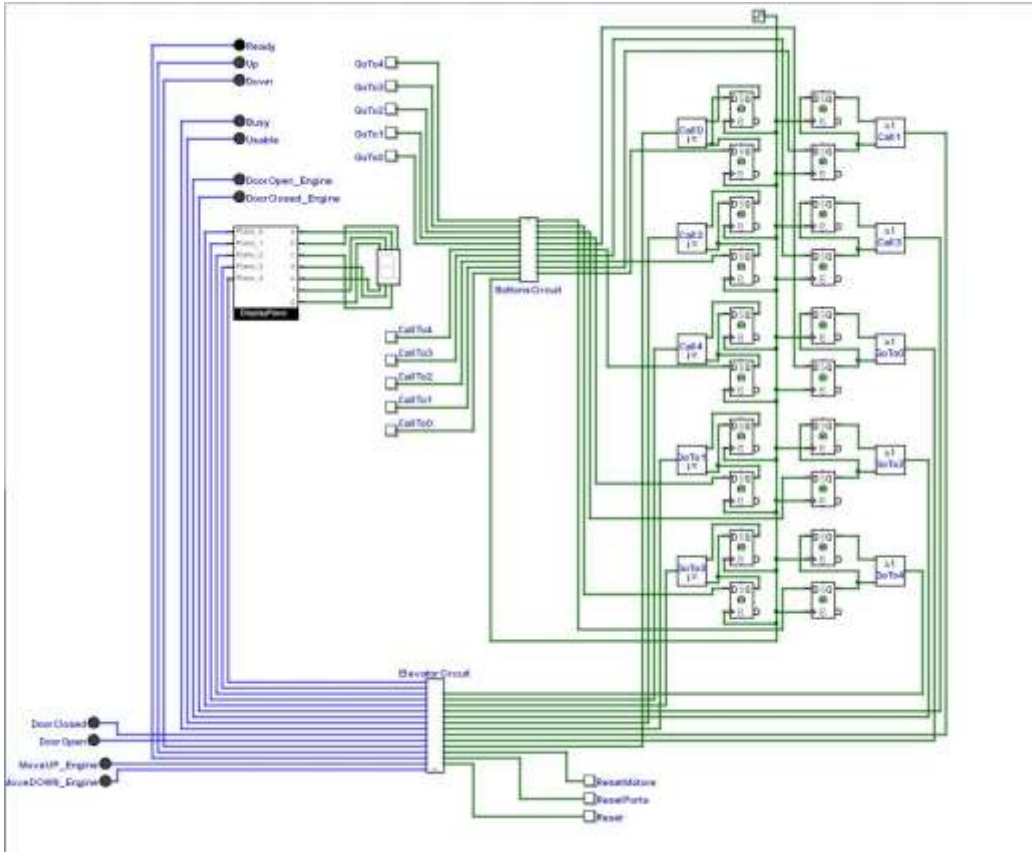
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity blinker_mod is
    Port (   clock1   : in    STD_LOGIC;
             ALLOUT   : out   STD_LOGIC_VECTOR (9 downto 0));
end blinker_mod;

architecture Behavioral of blinker_mod is
   SIGNAL   MainClk     : STD_LOGIC          := '0';          -- internal clock
   SIGNAL   MainCounter : UNSIGNED           (16 DOWNTO 0);   -- count range from 0 to 131071 (2^16)
   SIGNAL   RESET       : STD_LOGIC          := '0';          -- currently not used

   type state_type is (ST0,ST1,ST2,ST3,ST4,ST5,ST6,ST7,ST8,ST9);
   attribute ENUM_ENCODING: STRING;
   attribute ENUM_ENCODING OF state_type: type is "0100000011 0100100011 0101100011 0000000011 0010000011 0000010011 0100010
   SIGNAL STATE: state_type := ST0;                          -- my type definition

begin

   COUNT: PROCESS(RESET,MainClk)
   BEGIN
      IF    (RESET = '1' or MainCounter >= "11100001010100000") THEN MainCounter <= (OTHERS => '0');  -- 110000 clock cycles
      ELSIF (RISING_EDGE(MainClk)) THEN MainCounter <= MainCounter + 1;
      END IF;
   END PROCESS COUNT;


   SLOW: PROCESS(MainClk)
   BEGIN
      -- pause for 1us = 10clk cycles with MAINCLK @ 10MHz
      IF    (MainCounter = "00000000000010100") THEN STATE <= ST1;   -- @ 20 clk cycle    TG transfer gate open
      ELSIF (MainCounter = "00000000000101010") THEN STATE <= ST2;   -- @ 21 clk cycle    PG photo gate open
      ELSIF (MainCounter = "00000000000111110") THEN STATE <= ST1;   -- @ 30 clk cycle    PG photo gate closed
      ELSIF (MainCounter = "00000000000111111") THEN STATE <= ST3;   -- @ 31 clk cycle    TG tranfer gate closed
      ELSIF (MainCounter = "00000000001000000") THEN STATE <= ST4;   -- @ 32 clk cycle    AG antiblooming gate open
      ELSIF (MainCounter = "00000000001101111") THEN STATE <= ST5;   -- @ 47 clk cycle    AG antiblooming gate closed
      END IF;
   END PROCESS SLOW;

MainClk <= clock1;
with STATE select
     ALLOUT <="0100000011" WHEN ST0,
              "0100100011" WHEN ST1,
              "0101100011" WHEN ST2,
              "0000000011" WHEN ST3,
              "0010000011" WHEN ST4,
              "0000010011" WHEN ST5,
              "0100010011" WHEN ST6,
              "0100000010" WHEN ST7,
              "0100011001" WHEN ST8,
              "1100000011" WHEN ST9,
              "0100000011" WHEN OTHERS;
end Behavioral;
```

FPGAs


Ready
Up
Down
Busy
Unable
DoorOpen_Engine
DoorClosed_Engine
GoTo4
GoTo3
GoTo2
GoTo1
GoTo0
CallTo4
CallTo3
CallTo2
CallTo1
CallTo0
ButtonsCircuit
ElevatorCircuit
DoorClosed
DoorOpen
ResetMotors
ResetPorts
Reset

FPGAs

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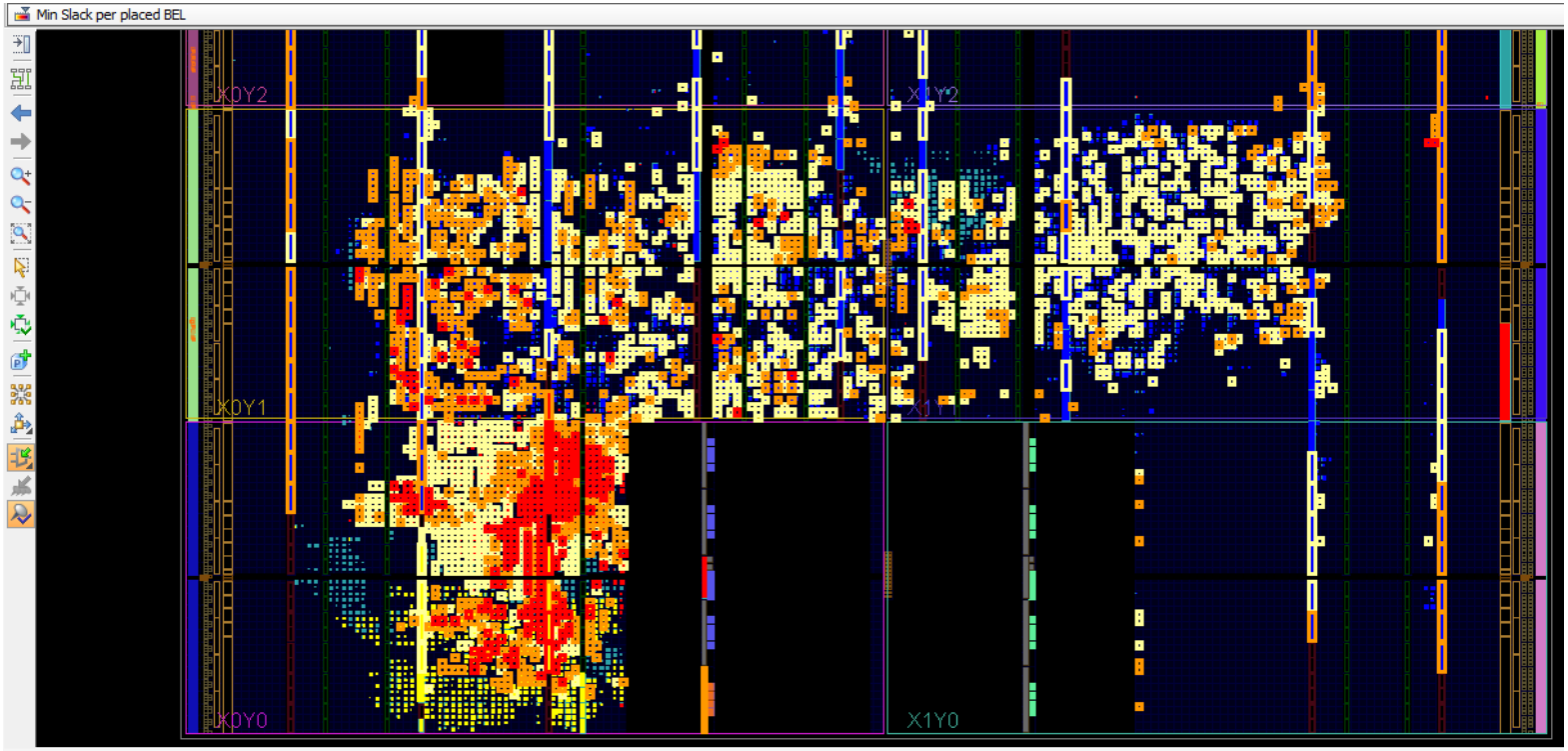

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FPGA

A Solução

Zynq-7000

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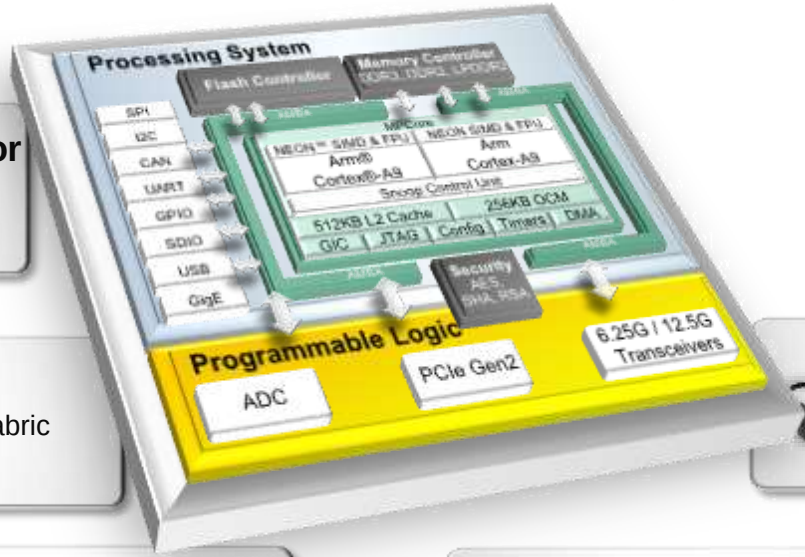
Single-Core
766MHz
Artix-7 FPGA Fabric

Dual-Core
800MHz
Artix-7 FPGA Fabric

Dual Core
1GHz
Kintex-7 FPGA Fabric



Application Processor
- Single or Dual Core
- Up to 1GHz

High BW Memory
- L1/L2 Cache, OCM
- DDR2/3, LPDDR2 w/ECC

FPGA Fabric
- 7 Series FPGA Fabric
- Custom Engines

Integrated Peripherals
- USB, GigE, CAN
- UART, SDIO, I2C, SPI

Tightly Coupled Domains
- 3000+ interconnects
- Up to 100Gb/s Bandwidth

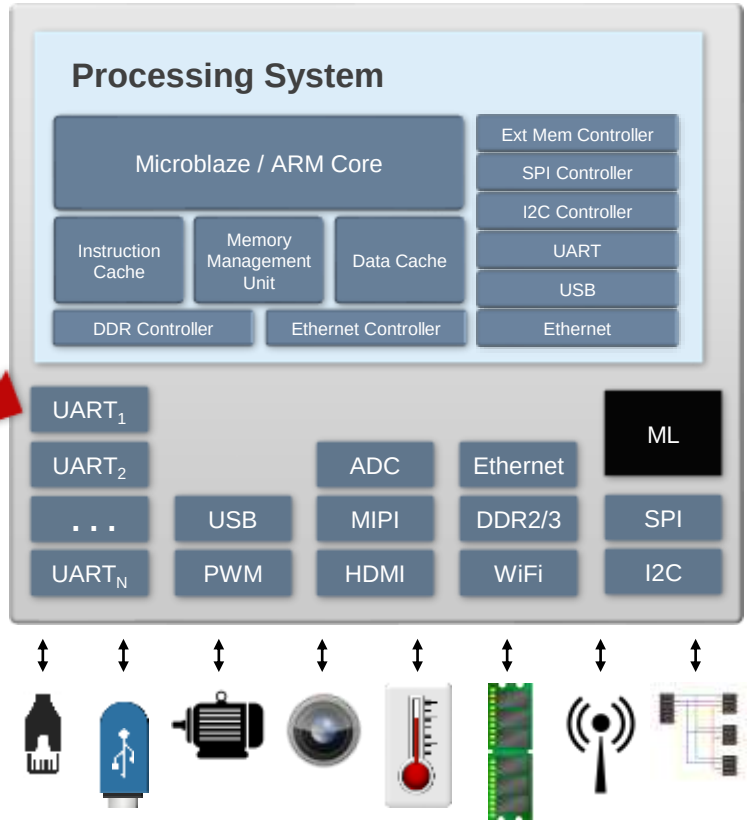
Integrated Analog
- Temp & Power Monitor
- 12-bit 1MSPS ADC

Mais periféricos?

Drag & Drop
100's de IP & Peripherals

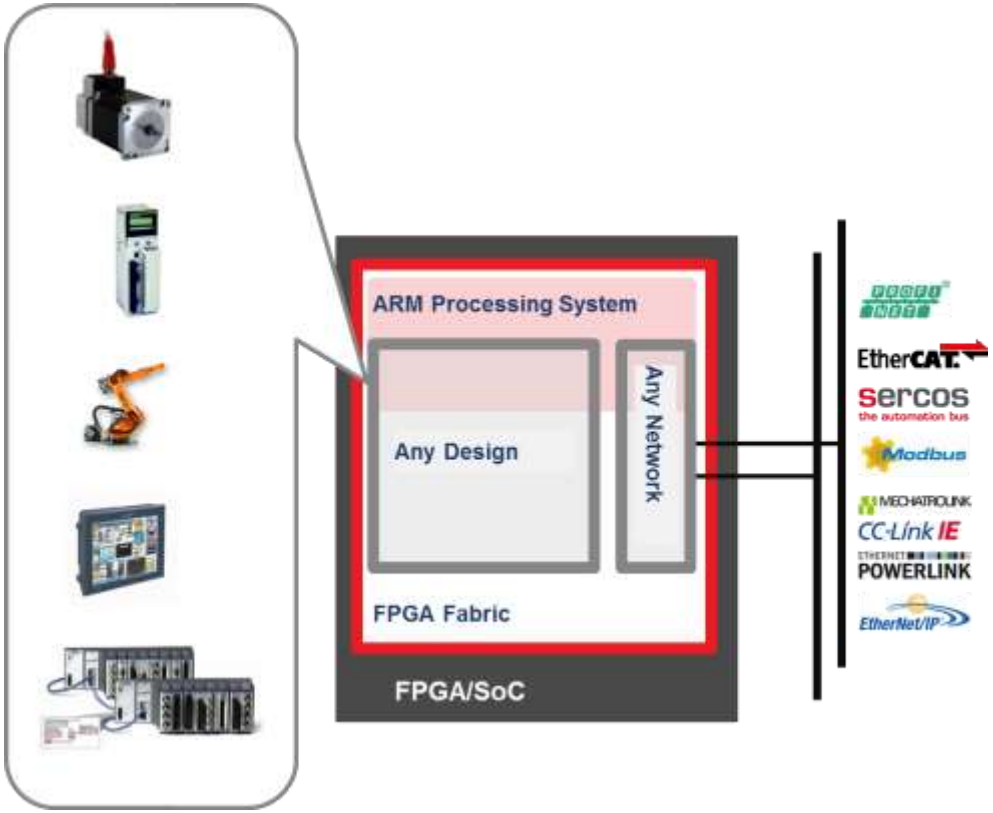
- IP Catalog
  - Partner IP
  - Automotive & Industrial
    - CAN
    - . . .
  - Embedded
  - Networking
  - Video & Image Processing
  - Digital Signal Processing

Drag, Drop, and Customize



- ✓ **Expanda** interfaces e features
- ✓ Adote os mais novos **protocolos**
  (e.g., EtherCAT, TSN, …)
- ✓ Desenvolva um sistema "**Future-Proof**" e que evolui de acordo com o mercado

Plataformas



Aceleração em Hardware

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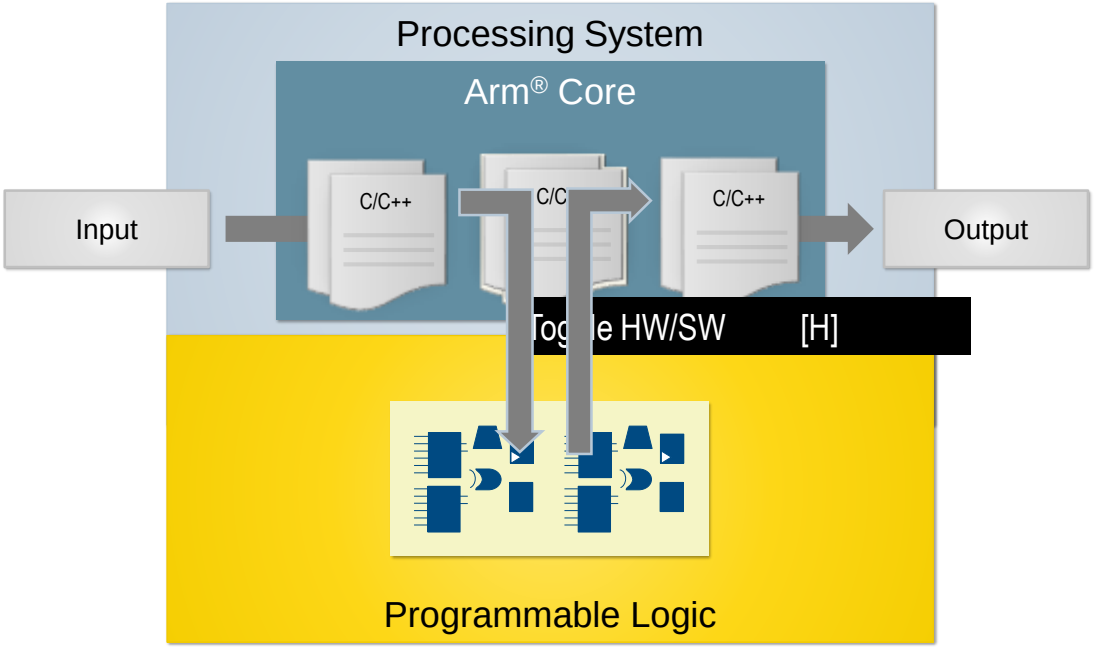
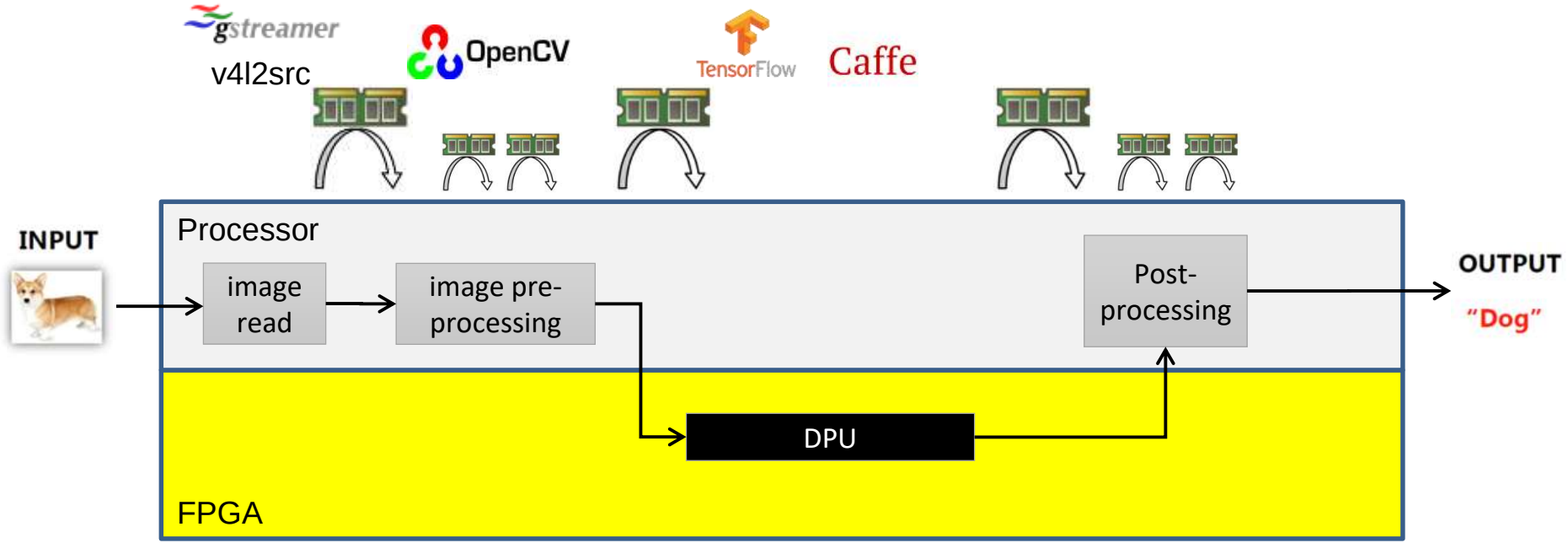
1. System-Level Profiling
2. Toggle SW-HW Partitioning
3. System Optimizing Compiler



Machine Learning with SoC/FPGA



OpenCV Support with Automatic HW Acceleration

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1. Cross-compile OpenCV application to Zynq (ARM A9/A53)
2. Profile and identify bottleneck functions
3. Minimal changes to the code and set functions to hardware. Compile for SW/HW.
4. Run on the board

OpenCV

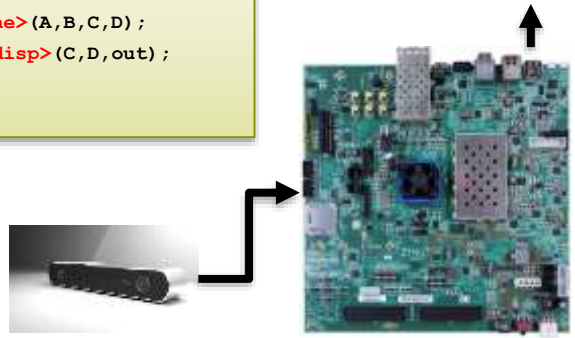
```
main(){
cv::imread(A);
cv::stereoRectify(A,B,C,D);
cv::stereoLBM(C,D,out);
cv::imshow(out);
}
```

Time [%]	Time
	4504 ms (100 %)
	4500 ms (100 %)
	4370 ms (97,1 %)
	4370 ms (97,1 %)
	3474 ms (77,2 %)
	3473 ms (77,2 %)
	3471 ms (77,2 %)
	3412 ms (75,8 %)
	2597 ms (57,7 %)
	2274 ms (50,5 %)
	1933 ms (43 %)
	1895 ms (42,1 %)
	1782 ms (39,6 %)
	1593 ms (35,4 %)
	1567 ms (34,8 %)
	1444 ms (32,1 %)

HW functions

Name	Clock Frequency (MHz)
stereoRectify	300
stereoLBM	300

```
main(){
cv::imread(A);
xF:stereoRectify<line>(A,B,C,D);
xF:stereoLBM<win,n_disp>(C,D,out);
cv::imshow(out);
}
```



xfOpenCV: 50+ Most Needed OpenCV Functions

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Basic Functionality	Geometric Transforms	Image Processing and Filters	Feature Detection and Classifiers	3D Reconstruction	Motion Analysis and Tracking
Absolute difference	Scale/Resize	Box	Canny edge detection	StereoLBM	Mean Shift Tracking (MST)
Accumulate	StereoRectify	Gaussian	Fast corner		LK Dense Optical Flow
Accumulate squared	Warp Affine	Median	SVM (binary)		
Accumulate weighted	Warp Perspective	Sobel	Harris corner		
Arithmetic addition	Remap	Custom convolution	Histogram of Oriented Gradients (HOG)		
Arithmetic subtraction		Equalize Histogram	Hough Lines		
Bitwise: AND, OR, XOR, NOT		Dilate			
Pixel-wise multiplication		Erode			
Channel combine		Bilateral			
Channel extract		OTSU Thresholding			
Color convert		Thresholding			
Convert bit depth		Image pyramid			
Table lookup		Color Detection			
		Integral image			
		Gradient Magnitude			
		Histogram			
		Gradient Phase			
		Min/Max Location			
		Mean & Standard Deviation			

Custom CV Function / Library Creation Flow

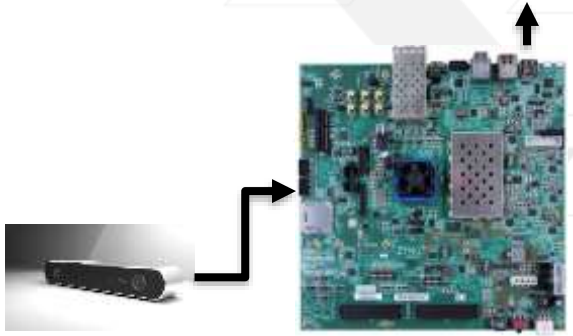
1. Cross-compile
2. Write custom CV function in C, C++
3. Assign functions to hardware. Compile using SDSoC
4. Run on the board

```
main(){
cv::imread(A);
xF:stereoRectify<line>(A,B,C,D);
xF:stereoLBM<win,n_disp>(C,D,E);
CUSTOM_CV(E,out);
cv::imshow(out);
}
```

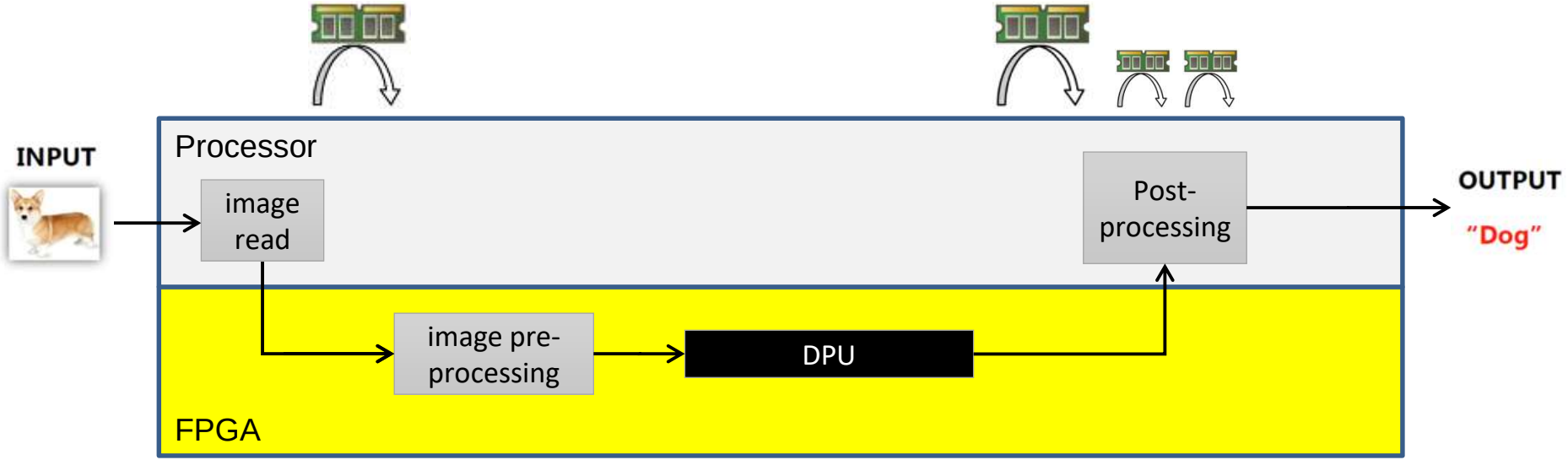
```
CUSTOM_CV(E,out){
  #pragma HLS PIPELINE
  for(…){
   #pragma HLS UNROLL
   for(…){ …
   }
  }
}
```

HW functions

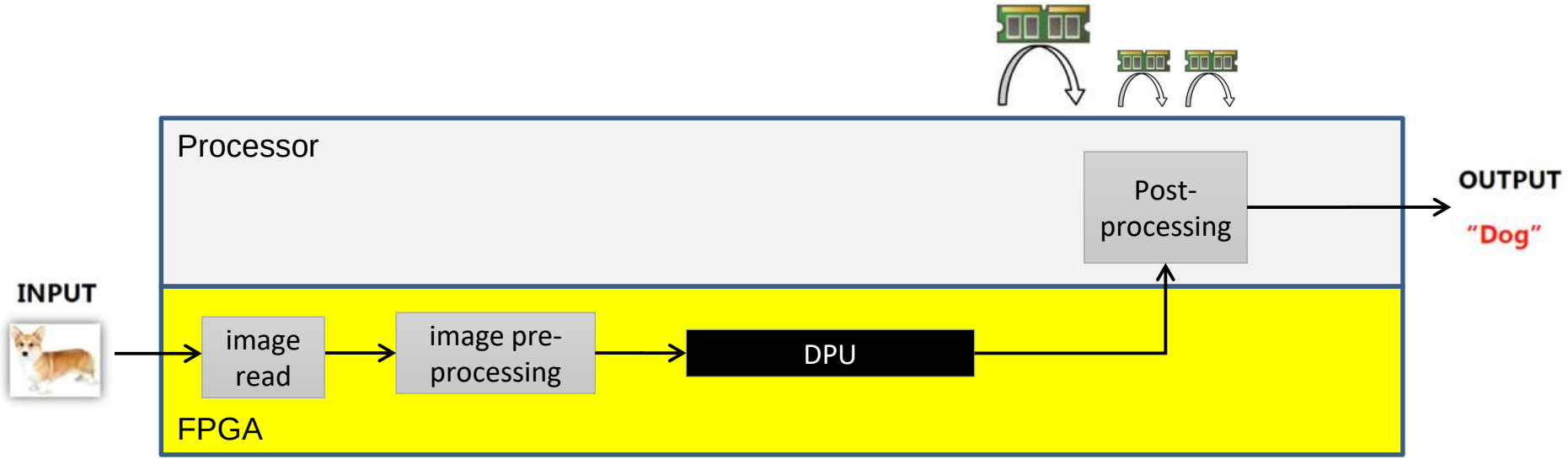
Name	Clock Frequency (MHz)
stereoRectify	300
stereoLBM	300
CUSTOM_CV	300



AI Computer Vision with SoC/FPGA



AI Computer Vision with SoC/FPGA



FPGAs - Brave New World

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